Multi-rate Digital Control with Interlacing and Its Application to Hard Disk Drives

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Abstract

This report presents a design method for a multi-rate digital controller with interlacing and its application to hard disk drives. The objective of this multi-rate controller design is to reduce the amount of real time computation. In general, a digital controller contains slow modes and fast modes. The slow-mode portion can be updated less frequently in order to reduce the computational load. In other words, one can decrease the sampling rate of the slow-mode controller. Hence, the resulting multi-rate digital controller is composed of a fast-mode controller with high sampling rate and a slow-mode controller with low sampling rate. The slow mode controller and the fast mode controller may be configured in either parallel form or serial form. The amount of computation is uniformly reduced by interlacing the slow-mode control outputs. This report also addresses two issues due to slow rate implementation of the slow-mode components: performance degradation and signal aliasing. The multi-rate control system is a linear periodically time-varying (LPTV) system. Using a lifting approach, the frequency response of the multi-rate system is represented by a frequency domain matrix. This matrix provides the information

to quantify the aliasing and the distortion effect in the multi-rate system. As an example of multi-rate control with interlacing, track-following control for hard disk drive is considered. Performance and aliasing analysis is presented for both the series and parallel structures. This design method for a multi-rate digital controller with interlacing is evaluated by both simulation and implementation results. The advantage of multi-rate control with interlacing is demonstrated.

I. Introduction

Multi-rate digital control has been a popular subject of research in the last two decades [1]–[4]. The digital control system may become multi-rate because it naturally involves more than one sampling period. An example is a motor control system with current, velocity and position feedback loops; the current loop is normally closed at the fastest rate. The control system becomes multi-rate if the control input is updated faster than the measurement sampling rate. Motivation for such multi-rate control is to make the control input smooth when the measurement sampling rate cannot be arbitrarily increased because of the sensor bandwidth or any other hardware constraint. The computer hard disk drive (HDD) is such an example [5], [6]. In the sectored servo system for HDD, a circular disk is divided into equally sized angular pieces (called sectors) and position information is written on the disk surface such that the position error signal (PES) is obtained once from each sector. While the numbers of sectors should be large for increased measurement sampling frequencies for PES and improved control performance, it should be kept small to reserve an ample space to store data on the disk. Gu and Tomizuka studied how the multi-rate control approach, which updates the controlling input faster the measurement sampling rate at a factor of N, may improve the control performance [6].

In this report, we study multi-rate control from the viewpoint of saving real time computation. In the implementation of control algorithms on consumer products such as hard disk drives, the

amount of computation for real time control should be kept minimal in order not to overload the digital signal processor or microprocessor, which may be a low end processor and may be performing various tasks in addition to real time control. We approach this problem by updating different components (modes) of the controller at different rates: fast modes at a fast rate and slow modes at a slow rate. Furthermore, slow modes are updated by interlacing them so that the amount of computation remains uniform from one time instance to another.

The remainder of this report is organized as follows. In Section II, the multi-rate digital control with interlacing is proposed by taking a single-rate track following controller for HDD as an example. The multi-rate control schemes are analyzed in Section III in frequency domain. In Section IV, the analytical results are applied to the HDD problem, and some simulation results are presented. Finally, experimental results are shown in Section V and conclusions are given in Section VI.

II. Multi-rate Digital Control with Interlacing

Dynamic controllers normally include slow dynamics and fast dynamics. For example, in PID (Proportional plus Integral plus Derivative) controller, we may regard that the I action represents slow dynamics or activities at relatively low frequencies, and the D action represents fast dynamics or activities at relatively high frequencies. If we decompose a digital control algorithm to the slow dynamic (low frequency) component and fast dynamics (high frequency) component, we may expect that we do not have to update the slow dynamics component as fast as the fast dynamics component.

As an example, we consider a digital controller designed for track following in a HDD application. The overall control system is as depicted in Fig. 1, and the zero order hold equivalent of the controlled plant (a suspension/carriage assembly driven by a voice coil motor (VCM) is

characterized by the frequency response in Fig. 2. The plant exhibits second order characteristics with several structural resonance modes. The gain plot is flat at low frequencies due to pivot friction [7]. The measurement sampling time is T_s = 99μs. The track following controller is described by

$$C_D(z) = 7.5e4 \frac{(z-0.9971)(z-0.9387)^2}{(z-0.9999)(z-0.9987)(z+0.2142)} \tag{1}$$

Note that this third order controller possesses two slow modes characterized by two poles at 0.9999 and 0.9987 and one fast mode characterized by a pole at -0.2142.

A. Parallel Decomposition and Serial Decomposition

By applying the partial fraction expansion to the controller Eq. (1), we obtain

$$\begin{aligned} C_D(z) &= C_{Ds1}(z) + C_{Ds2}(z) + C_{Df}(z) + K_D \\ &= \frac{5.19e2}{z-0.9999} + \frac{-2.75e2}{z-0.9987} + \frac{-8.20e4}{z+0.2142} + 7.5e4 \end{aligned} \tag{2}$$

The controller can be implemented as shown in Fig. 3. Notice that in this configuration, the slow dynamics blocks and fast dynamics block are in parallel, and we call the decomposition in Eq. (2) a parallel decomposition. In view of the slow dynamics of the first two terms in the right hand side of Eq. (2), if we implement them at the lower sampling rate, the controller becomes as depicted in Fig. 4. Note that the constant gain K_D is combined to $C_{Df}(z)$.

In Fig. 4, $\downarrow$2 denotes down sampling by the factor of 2. Assume that the measurement sampling rate is high enough so that the down sampling will not introduce serious aliasing. Each controller block implemented at the lower sampling rate is obtained by assuming that $PES(k+1)$ remains the same as $PES(k)$: i.e. the down sampler is followed by a zero order hold and noting the following relation.

Lemma 1: Given a first order discrete time block $1/(z-a)$, if its input is held constant for N time steps, the transfer function at a slower sampling rate by a factor of N is

$$\frac{a^{N-1}+a^{N-2}+\cdots+a+1}{z^N-a^N} \tag{3}$$

Proof: This relation is easily obtained by first converting the original first order block to a state-space form, i.e. $x(k+1)=ax(k)+u(k)$, $y(k)=x(k)$ and noting

$$x(k+N)=a^N x(k)+(a^{N-1}+a^{N-2}+\cdots+a+1)u(k)$$

for $u(k)=u(k+1)=\cdots=u(k+N-1)$ ■

By updating the slow modes of the controller at lower rates, the total amount of computation may be reduced. In the implementation in Fig. 4, however, the amount of computation at instances of down sampling is essentially the same as the original single rate digital controller while it is reduced between two adjacent down sampling instances. The non-uniform nature of amount of computation is not quite attractive from practical point of view. If we are to utilize multi-rate control for reducing the amount of real time computation, such a reduction must be nearly uniform among all time instances. For the third order controller under consideration, the uniformity may be achieved by interlacing the two slow mode blocks at even and odd time instances as shown in Fig. 5. The output of each block of the controller may look as shown in the time chart in Fig. 6.

The controller transfer function Eq. (1) can be decomposed into serial form as shown below.

$$C_D(z)=C_{Ds}(z)\cdot C_{Df}(z) \tag{4}$$

where

$$C_{Ds}(z) = C_{Ds1}(z) + C_{Ds2}(z) + K_D$$
$$= \frac{1.027e4}{z - 0.9999} + \frac{-0.555e4}{z - 0.9987} + 7.5e4 \quad (5)$$
$$C_{Df}(z) = \frac{z - 0.9387}{z + 0.2142} \quad (6)$$

Noting that the gain factor $7.5e4$ in $C_{Ds}(z)$, but it could have been distributed to $C_{Ds}(z)$ and $C_{Df}(z)$. Fig. 7 shows the diagram for implementation of this serial decomposition. Noting that $C_{Ds}(z)$ represents the slow dynamics, it is expected that we may implement this part at slower rate without losing performance. By implementing $C_{Ds}(z)$ at a rate slower than for $C_{Df}(z)$ by a multi-rate ratio of 2 and letting two slow dynamics blocks interlace, we obtain the implementation diagram in Fig. 8. In the figure, the R blocks represent interpolators using repetition which convert the signal from slow rate to fast rate. Notice that from the view point of computation, the amount of real time computation for implementing the third order controller Eq. (1) in the proposed multi-rate schemes with interlacing is equivalent to that for implementing a single-rate second order digital controller. In the next section, we will examine these multi-rate schemes in both the time domain and frequency domain to compare their performance to the original single-rate controller.

B. Some Generalization

The multi-rate digital control with interlacing that we proposed in the previous subsection may be generalized in several ways. In this subsection, we consider multi-rate implementations of single-rate digital controllers expressed in the form

$$C_D(z) = K_D \frac{\prod_{k=1}^{m_1}(z - z_k)\prod_{l=1}^{m_2}(z - z_l)(z - \tilde{z}_l)}{\prod_{i=1}^{n_1}(z - p_i)\prod_{j=1}^{n_2}(z - p_j)(z - \tilde{p}_j)} \quad (7)$$

where $n_1 + 2n_2 = m_1 + 2m_2 = n_c$ and n_c is the order of the controller. Note that the digital controller obtained by digital redesign of analog controllers is expressed in this form [8], [9]. Assume that the (fast) sampling period for Eq. (7) is T_s and that there are no poles outside of the unit circle. The slow sampling rate and the multi-rate ratio should be selected by the distribution of all poles in Eq. (7), but let us assume here that the multi-rate ratio is N. Then, a rule of thumb may be developed to classify the poles to slow modes and fast modes. Under the above stated assumption, the Nyquist frequency for the lower sampling rate is given by

$$\omega_N = \frac{\pi}{NT_s} \tag{8}$$

We will consider any mode involved in Eq. (7) be slow and the slow sampling rate is adequate if the modal frequency is below the Nyquist frequency given by Eq. (8) by a factor of five: i.e. the critical frequency is

$$\omega_c = \frac{\omega_N}{5} \tag{9}$$

Let us now represent each of positive real poles in Eq. (7) as

$$p_i = e^{-\omega_{ni} T_s} \tag{10}$$

Rule 1: p_i is considered to represent a slow mode if $\omega_{ni} \leq \omega_c$. Notice that all negative real poles represent fast modes.

Each pair of complex conjugate poles are expressed as

$$p_j = r_j e^{j\theta_j}, \quad \tilde{p}_j = r_j e^{-j\theta_j} \tag{11}$$

where

$$r_j = e^{-\zeta_j \omega_{nj} T_s}, \quad \theta_j = \omega_{nj} T_s \sqrt{1 - {\zeta_j}^2} \tag{12}$$

Rule 2: p_j and $\tilde{p}_j$ represent slow modes if $\omega_{nj} \leq \omega_c$.

Rule 1 and Rule 2 mean that poles located inside the hatched region in Fig. 9 represent slow modes and all other poles inside or on the unit circle represent fast modes.

After grouping controller poles into the slow and fast modes, the controller transfer function may be represented as

$$C_D(z) = C_{Ds}(z) + C_{Df}(z) \tag{13}$$

in case of parallel decomposition, or

$$C_D(z) = C_{Ds}(z) \cdot C_{Df}(z) \tag{14}$$

in case of serial decomposition. The further development to implement Eq. (13) or Eq. (14) as a multi-rate controller with interlacing follows the procedure as explained in Section II-A. When multi-rate ratio N is large, the power spectrum of the disturbances and PES could probably contain major components in the frequency region above the Nyquist frequency of slow sampling rate. Adding a low pass filter before the down sampler is a good way to filter out the high frequency components to prevent aliasing. Although some computation may be introduced by adding low pass filter, the amount is relatively small compared to that saved by multi-rate control with interlacing.

III. Analysis of Multi-rate Controller with Interlacing

The multi-rate control system is a linear periodically time-varying (LPTV) system. One method to describe LPTV systems is to use a frequency domain lifting technique such that the frequency response of the LPTV system can be represented by a frequency domain matrix [10]. Based on the information in the frequency response matrix, a measure can be obtained to quantify the aliasing effect. If aliasing is negligible, we can approximate it by a linear time invariant (LTI) system [11]. Some key results of the frequency response of LPTV systems are reviewed

Some key results of the frequency response of LPTV systems are reviewed. In the remainder of this section, the aliasing in the multi-rate controller with interlacing is studied. Aliasing is presented due to the down sampling operation in the slow-rate implementation. It is shown that the aliasing level is small base on the assumption that the measurement sampling rate is fast enough so that the down sampling will not introduce serious aliasing. The performance analysis of the multi-rate controller is also considered.

A. Frequency Domain Representation of LPTV Systems

The concept of frequency response for LPTV systems is defined in [10], [12]. Assume an LPTV system with input $x(k)$, output $y(k)$ and period P is given by

$$y(k) = \sum_{l=-\infty}^{\infty} f(k,l)x(l) \tag{15}$$

where $f(k,l)$ is the response of the system at time k to a unite impulse at time l and $f(k,l) = f(k+P, l+P)$. By defining $h(l,k) = f(k+l,l)$, the P-periodic condition gives $h(l,k) = h(l+P,k)$. Equation (15) can be rewritten as

$$\begin{aligned} y(k) &= \sum_{i=-\infty}^{k} h(i,k-i)x(i) \\ &= \sum_{l=0}^{P-1}\sum_{r=-\infty}^{\infty} h(l,k-(Pr+l))x(Pr+l) \end{aligned} \tag{16}$$

Define the LTI system $H^l(z) = \sum_{k=0}^{\infty} h(l,k)z^{-k}$, and due to periodicity P, $H^l = H^{l+P}$. Then the LPTV system can be represented by P LTI systems H^l with a switch in the output as shown in Fig. 10 [13]. The switch is connected to H^l at sampling time $Pk+l$.

By lifting the input and output sequences into vectors of length P

$$\underline{y}(k) = \begin{bmatrix} y(Pk) & y(Pk+1) & \cdots & y(Pk+P-1) \end{bmatrix}^T$$

$$\underline{x}(k) = \begin{bmatrix} x(Pk) & x(Pk+1) & \cdots & x(Pk+P-1) \end{bmatrix}^T$$

This system can be represented using an equivalent LTI system H which has P inputs and P outputs

$$\underline{Y}(z^P) = H(z^P)\underline{X}(z^P) \tag{17}$$

with

$$H(z^P) = \begin{bmatrix} H_0^0(z^P) & z^{-P}H_{P-1}^1(z^P) & \cdots & z^{-P}H_1^{P-1}(z^P) \\ H_1^0(z^P) & H_0^1(z^P) & \cdots & z^{-P}H_2^{P-1}(z^P) \\ \vdots & \vdots & \ddots & \vdots \\ H_{P-1}^0(z^P) & H_{P-2}^1(z^P) & \cdots & H_0^{P-1}(z^P) \end{bmatrix} \tag{18}$$

where $\underline{Y} = \begin{bmatrix} Y_0(z^P) & Y_1(z^P) & \cdots & Y_{P-1}(z^P) \end{bmatrix}^T$ is the $\mathcal{Z}$-transform of the vector sequence $\underline{y}$, and $\underline{X}$ is similarly defined for $\underline{x}$. $H_k^l(z^P)$'s are the polyphase components of $H^l(z)$

$$H^l(z) = \sum_{k=0}^{P-1} z^{-k}H_k^l(z^P) \tag{19}$$

Equation (17) and (18) represent the time domain lifted system.

As shown in [12], the expression for the input-output relation in frequency domain can be written as

$$Y(z) = G_0(z)X(z) + \sum_{n=1}^{P-1} G_n(z)X(z\phi^n) \tag{20}$$

where $\phi = e^{j2\pi/P}$. The lifted system in time domain and that in frequency domain are connected through

$$G_n(z) = \frac{1}{P}\sum_{i=0}^{P-1}\sum_{j=0}^{P-1} \phi^{jn} z^{j-i} H_{(i,j)}(z^P) \tag{21}$$

where $H_{(i,j)}(z^P)$ denotes the entry in row i, column j of the matrix $H(z^P)$. Note that in the Eq. (20), the output spectrum is the sum of the shaped versions of frequency shifted input spectrum, $X(z\phi^n)$. If $G_1(z) = \cdots = G_{P-1}(z) = 0$, then the aliasing is absent. Therefore, $G_n(z)|_{n=1,\cdots,P-1}$

give a measure of the aliasing effect in an LPTV system [11]. Moreover, the frequency spectrum of the input signal also affects the level of aliasing.

Equation (20) can be written in a matrix form.

$$\underline{\hat{Y}}(z) = \begin{bmatrix} G_0(z) & G_1(z) & \cdots & G_{P-1}(z) \\ G_{P-1}(z\phi) & G_0(z\phi) & \cdots & G_{P-2}(z\phi) \\ \vdots & \vdots & \ddots & \vdots \\ G_1(z\phi^{P-1}) & G_2(z\phi^{P-1}) & \cdots & G_0(z\phi^{P-1}) \end{bmatrix} \underline{\hat{X}}(z)$$

$$= G^{FR}(z)\ \underline{\hat{X}}(z) \tag{22}$$

where $\underline{\hat{Y}}(z) = [Y(z)\ Y(z\phi)\ \cdots\ Y(z\phi^{p-1})]^T$, and $\underline{\hat{X}}(z)$ is similarly defined. In Eq. (22), $G^{FR}(z)$ is called the frequency response matrix of the LPTV system [10], [11]. It is obvious that the frequency response matrix for a LTI system, $Y(z) = G_0(z)U(z)$, is in diagonal form

$$\underline{\hat{Y}}(z) = \begin{bmatrix} G_0(z) & 0 & \cdots & 0 \\ 0 & G_0(z\phi) & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & G_0(z\phi^{P-1}) \end{bmatrix} \underline{\hat{X}}(z) \tag{23}$$

The frequency response matrix transforms the LPTV system to a multi-input, multi-output LTI system. This description is used as an analysis tool in the following sections.

B. Multi-rate Digital Control with Interlacing

The main purpose of the multi-rate controller discussed is to save real-time computation. The multi-rate controller is designed from a single-rate digital controller. The slow-mode and fast-mode components of the single-rate controller are separated according to the locations of poles. The slow-mode controller is implemented at slow rate. Furthermore, the slow-mode controller is

decomposed to several elements and updated at different fast sampling time instances. Therefore, the amount of computation is uniformly reduced among all time instances. There are two kinds of multi-rate controller structures. In the parallel structure, the slow part and fast part are connected in parallel while in the serial structure the slow part is followed by the fast part. In this section, the multi-rate digital control systems are represented using frequency response matrices. The aliasing effect presents in the multi-rate controller due to down sampling is evaluated. The system performance for disturbance rejection is also considered. To simplify the discussion, we consider a multi-rate controller with a multi-rate ratio of 2. Furthermore, the slow part of the controller has been decomposed into two blocks and are interlaced.

1) Parallel Structure: Fig. 11 shows the multi-rate controller implemented in parallel form [14]. The output of the slow mode controller at even sampling time $2k$ is related to its input by

$$\begin{aligned} u_s(2k) &= u_1(2k) + u_2(2k-1) \\ &= C_{Ds1}(z^2)e(2k) + C_{Ds2}(z^2)e(2k-1) \end{aligned} \tag{24}$$

while at odd sampling time $2k+1$

$$\begin{aligned} u_s(2k+1) &= u_1(2k) + u_2(2k+1) \\ &= C_{Ds1}(z^2)e(2k) + C_{Ds2}(z^2)e(2k+1) \end{aligned} \tag{25}$$

Equations (24) and (25) show that this multi-rate controller is a periodic system with a period of 2. Since the multi-rate controller makes the system a LPTV system, the analysis method discussed in the Section III-A can be used to analyze this multi-rate system.

From Eq. (24) and (25), the lifted input and output signal for the slow part are related by

$$\underline{U_s}(z^2) = \begin{bmatrix} C_{Ds1}(z^2) & z^{-2}C_{Ds2}(z^2) \\ C_{Ds1}(z^2) & C_{Ds2}(z^2) \end{bmatrix} \underline{E}(z^2) \tag{26}$$

Notice that the slow-mode controller input $\underline{E}(z^2)$ and output $\underline{U_s}(z^2)$ correspond to $\underline{X}(z^P)$ and $\underline{Y}(z^P)$ respectively in Eq. (17).

The overall controller can be expressed in switch structure as shown in Fig. 10. $H^0(z)$ and $H^1(z)$ are obtained from Eq. (18), (19) and (26).

$$H^0(z) = \left(C_{Ds1}(z^2) + z^{-1}C_{Ds1}(z^2)\right) + C_{Df}(z) \tag{27}$$

$$H^1(z) = \left(C_{Ds2}(z^2) + z^{-1}C_{Ds2}(z^2)\right) + C_{Df}(z) \tag{28}$$

The additional term $C_{Df}(z)$ comes from the fast-mode controller branch. The controller input error signal is connected to $H^0(z)$ at even time instants and to $H^1(z)$ at odd time instants. This gives us a better insight of how the multi-rate controller works.

For the frequency analysis, it is more convenient to represent the lifted controller in frequency domain. According to Eq.(21) and (26), the frequency response matrix for the slow part is

$$C_s^{FR}(z) = \begin{bmatrix} G_{s0}(z) & G_{s1}(z) \\ G_{s1}(-z) & G_{s0}(-z) \end{bmatrix} \tag{29}$$

where

$$\begin{aligned} G_{s0}(z) &= \frac{1}{2}(H_{(0,0)}(z^2) + zH_{(0,1)}(z^2) \\ &\quad + z^{-1}H_{(1,0)}(z^2) + H_{(1,1)}(z^2)) \\ &= \frac{1}{2}(1 + z^{-1})(C_{s1}(z^2) + C_{s2}(z^2)) \end{aligned} \tag{30}$$

$$\begin{aligned} G_{s1}(z) &= \frac{1}{2}(H_{(0,0)}(z^2) - zH_{(0,1)}(z^2) \\ &\quad + z^{-1}H_{(1,0)}(z^2) - H_{(1,1)}(z^2)) \\ &= \frac{1}{2}(1 + z^{-1})(C_{s1}(z^2) - C_{s2}(z^2)) \end{aligned} \tag{31}$$

For the fast-mode component, LTI transfer function $C_{Df}(z)$ is written in matrix form

$$C_f^{FR}(z) = \begin{bmatrix} C_{Df}(z) & 0 \\ 0 & C_{Df}(-z) \end{bmatrix} \tag{32}$$

Hence, the overall controller is expressed as

$$C^{FR} = \begin{bmatrix} C_0(z) & C_1(z) \\ C_1(-z) & C_0(-z) \end{bmatrix} = C_s^{FR}(z) + C_f^{FR}(z) \tag{33}$$

Notice that the aliasing component in the controller is obtained from

$$C_1(z) = G_{s1}(z) \tag{34}$$

2) Serial Structure: Figure 12 shows the multi-rate controller implemented in series form. If the controller is represented in switch structure in Fig. 10, H^0 and H^1 are given by

$$H^0(z) = \left(C_{Ds1}(z^2) + z^{-1}C_{Ds1}(z^2)\right) C_{Df}(z) \tag{35}$$

$$H^1(z) = \left(C_{Ds2}(z^2) + z^{-1}C_{Ds2}(z^2)\right) C_{Df}(z) \tag{36}$$

For the frequency domain analysis, the fast part and slow part expressions are the same as that of the parallel case except that there is an additional constant gain K_D in $G_{s0}(z)$. The overall controller is expressed as

$$C^{FR} = \begin{bmatrix} C_0(z) & C_1(z) \\ C_1(-z) & C_0(-z) \end{bmatrix} = C_f^{FR}(z)\ C_s^{FR}(z) \tag{37}$$

Also the aliasing component is

$$C_1(z) = 0.5(1 + z^{-1})C_{Df}(z)\left(C_{Ds1}(z^2) - C_{Ds2}(z^2)\right) \tag{38}$$

Notice that the multi-rate implementation results in a low-pass filter $0.5(1 + z^{-1})$ in $C_1(z)$. This low-pass filter helps to reduce the signal aliasing at high frequencies.

3) Performance of the Multi-rate Control System: If the aliasing effect is small, then the multi-rate controller can be best approximated by the LTI system $C_0(z)$. Therefore, the output sensitivity function for disturbance rejection is given by

$$S(z) = (I + P(z)\ C_0(z))^{-1} \tag{39}$$

where $P(z)$ is the ZOH equivalent of the controlled plant. If the aliasing effect is not negligible, we can use the frequency response matrix to model the controller and the plant. Hence, the overall system becomes a enlarged MIMO system. Its performance can be evaluated using MIMO system analysis methods.

IV. Example: HDD Track Following Control

In this section, we present the analysis of multi-rate control systems in the frequency domain for the hard disk drive system and the controller design presented in Section II.

For parallel implementation, the multi-rate controller consists of

$$\begin{aligned} C_{Ds1}(z^2) &= \frac{1038}{z^2 - 0.9999} \\ C_{Ds2}(z^2) &= \frac{-549.2}{z^2 - 0.9974} \\ C_{Df}(z) &= 75000\frac{z - 0.879}{z + 0.2142} \end{aligned} \tag{40}$$

while for serial implementation,

$$\begin{aligned} C_{Ds1}(z^2) &= \frac{2.05e4}{z^2 - 0.9999} \\ C_{Ds2}(z^2) &= \frac{-1.11e4}{z^2 - 0.9974} \\ C_{Df}(z) &= \frac{z - 0.9387}{z + 0.2142} \\ K_D &= 75000 \end{aligned} \tag{41}$$

A. Frequency Domain Analysis

1) Aliasing effect in the controller: From the frequency response matrix, the input-output relation of the controller is given by

$$U(z) = C_0(z)E(z) + C_1(z)E(-z) \tag{42}$$

To quantify the aliasing in the controller, we use the ratio of $C_1(z)$ to $C_0(z)$ as a measure of aliasing.

$$A(z) = C_1(z)/C_0(z) \tag{43}$$

Figure 13 shows how aliasing may present in parallel and series implementations of the multi-rate controller. Notice that aliasing may be more serious in the series case in this example. The effect of aliasing depends on $C_1(z)$ as well as high frequency components in the error signal $E(z)$ above the Nyquist frequency corresponding to the slow sampling rate (2,500 Hz in this example). Thus, it is important to check these two aspects in the multi-rate implementation and to make it sure the aliasing term $C_1(z)E(-z)$ is negligible.

2) Performance analysis: If the aliasing effect is negligible, the sensitivity function of the multi-rate system can be calculated from Eq.(39). The frequency responses of the sensitivity functions for the multi-rate system with parallel and serial structures are shown in Fig. 14 and Fig. 15. From the performance comparison in the figures, it is observed that the performance of the multi-rate systems in this example is close to that of the original single fast rate system.

B. Time Domain Simulation

Using the simulated hard disk drive servo system and the controller described in Section IV, time domain responses are simulated in the presence of disturbances including windage torque, servo written-in position error, disk vibration and sensor noise, which enter the system

TABLE I

PERFORMANCE COMPARISON

Scheme	Case 1: 3σ(%track)	Case 2: 3σ(%track)
Single-rate	5.2461	7.3632
MR parallel	5.2827	8.1282
Degradation	0.7%	10.4%
MR series	5.4026	12.2649
Degradation	3.0%	66.5%

as depicted in Fig. 1. Their power spectral density plots are shown in Fig. 16. Time plots of PES for the systems using single-rate controller, multi-rate controller in parallel form and series form are given in Fig. 17 (a), (b) and (c). These simulation results are used as a reference. In the next set of simulations, we introduce an additional large amplitude disturbance above the slow rate Nyquist frequency and investigate the effect of aliasing. Note that this disturbance is artificial and does not exist in real HDD systems. The additional disturbance is an output sinusoidal disturbance $d(k)$ with magnitude 0.04 and frequency $4,800Hz$. Figures 17 (d), (e) and (f) show the PES plots for the single-rate and multi-rate controllers with the additional disturbance $d(k)$.

The performance of a controller in time domain is evaluated based on the TMR which is the 3 times standard deviation (3σ) of PES. In Table I, case 1 is the simulation without $d(k)$. The multi-rate controllers can achieve nearly the same performance of the single-rate controller. When the additional disturbance is added in case 2, the 3σ value is increased by 10.4% using parallel multi-rate controller and by 66.5% using series multi-rate controller. The performance deterioration in the multi-rate system is caused by the serious aliasing effect which comes from

$d(k)$. The results are consistent to the analytical predication shown in Fig. 13.

V. Experimental Results

The experimental setup for HDD single-stage track following control is shown in Fig. 18. The position error is measured by a Laser Doppler Vibrometer (LDV). A floating point DSP (TMS230C67X) is used for controller implementation. The LDV displacement output is sampled by DSP with sampling frequency $50kHz$. Therefore, the fast-mode controller is implemented at $T_{fast} = 1/50kHz$, while the slow-mode controller at $T_{slow} = 1/25kHz$, i.e. the multi-rate ratio is 2. The controlled plant is characterized by the frequency response in Fig. 19. The track following controller is described by

$$C_D(z) = 1.0882\frac{(z-0.9813)(z-0.9681)(z+1)}{(z-0.9999)(z-0.8496)(z-0.6137)} \tag{44}$$

Figure 20 shows the PES time plots for original single fast rate control system and the multi-rate control with interlacing using parallel decomposition and serial decomposition. The performance of a controller in time domain was evaluated based on the 3 times standard deviation (3σ) of PES. From Table II, the 3σ value only increased by 1.7% for parallel decomposition case and by 4.7% for serial decomposition case. The performance is slightly deteriorated using multi-rate control with interlacing while the amount of computation has been reduced.

VI. Conclusions

Multi-rate control with interlacing has been proposed as a means to reduce the amount of real time computation in the implementation of digital control algorithms on DSP or microprocessors. The original single-rate digital controller is decomposed into two parts: one represents slow modes and the other fast modes. The part representing slow modes is implemented at a low

TABLE II

PERFORMANCE COMPARISON

Scheme	Fast Rate	MR parallel	MR serial
3σ (nm)	49.94	50.82	52.32
Degrade %	-	1.7%	4.7%

sampling rate; furthermore it is decomposed into multiple blocks and those blocks are interlaced to uniformly reduce the amount of real time computation. A third order track following controller for HDD has been used as an example throughout the report.

Performance and aliasing effect have been studied for multi-rate control for saving of computations. Using the frequency domain lifting technique, frequency response matrices were used to analyze the multi-rate system. The aliasing effect due to down sampling in the multi-rate controller depended on off-diagonal elements of the frequency response matrices and the error signal, which is the input to the controller. Analysis methods were applied to the HDD example to quantify the aliasing effect and performance. Finally, both frequency domain analysis and experimental results verified that the performance is maintained using the proposed multi-rate control with interlacing while the computation has been reduced.

ACKNOWLEDGMENT

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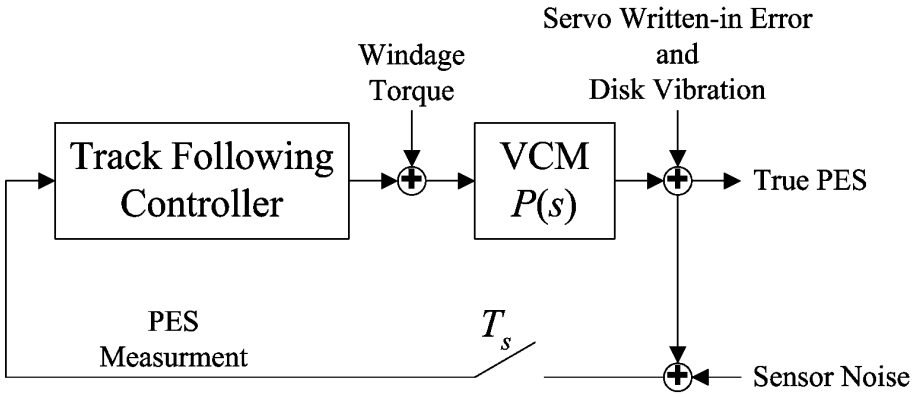

Fig. 1. HDD track-following servo system with disturbances

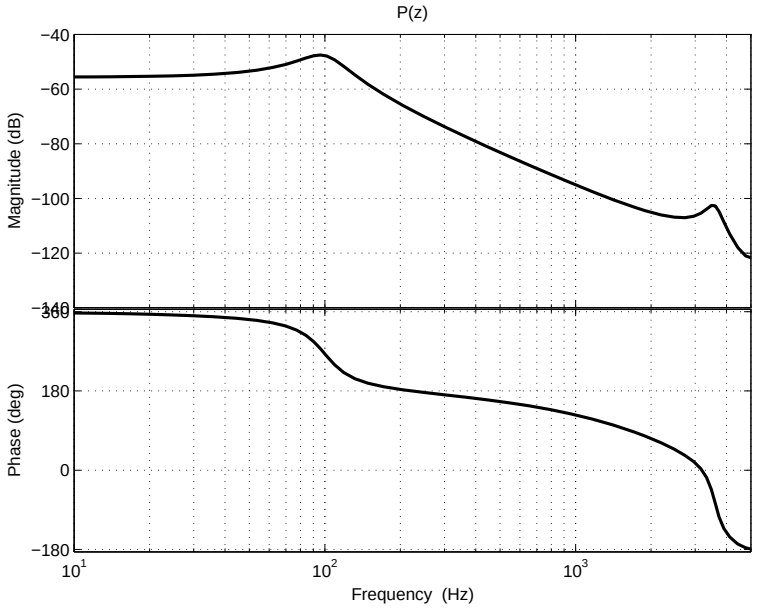

Fig. 2. Frequency response of VCM $P(z)$ (simulation)

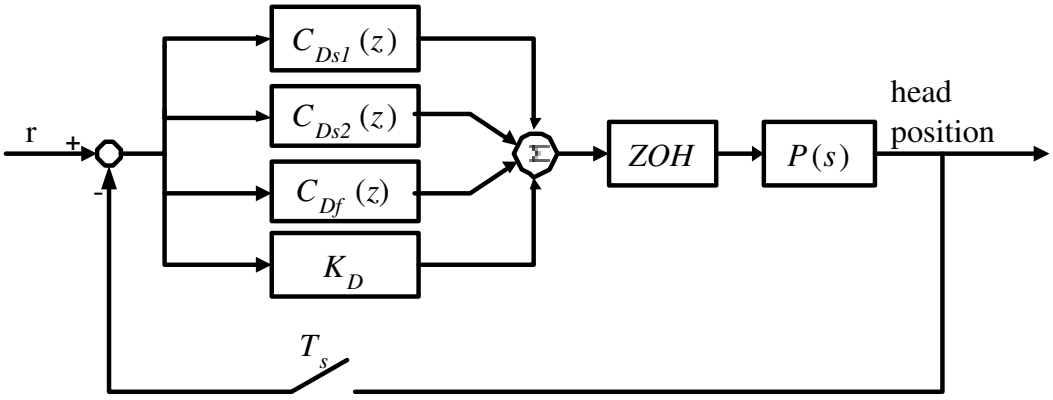

Fig. 3. Implementation of controller using parallel decomposition

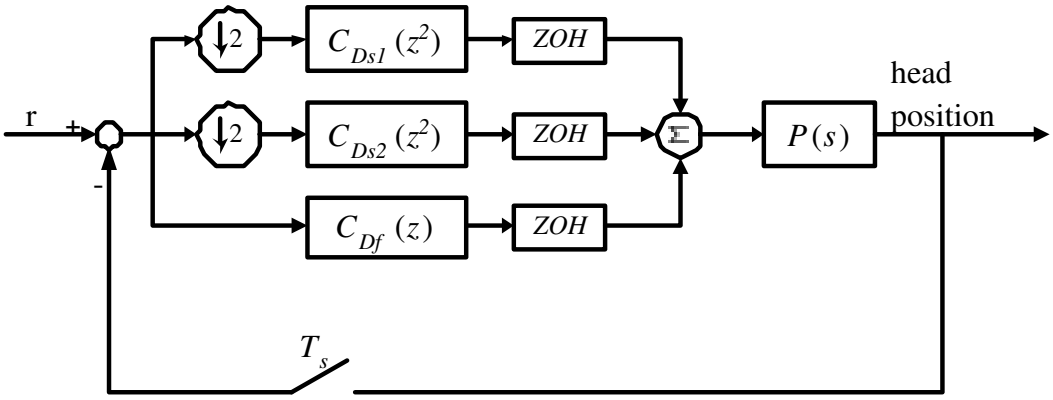

Fig. 4. Block diagram of multi-rate control

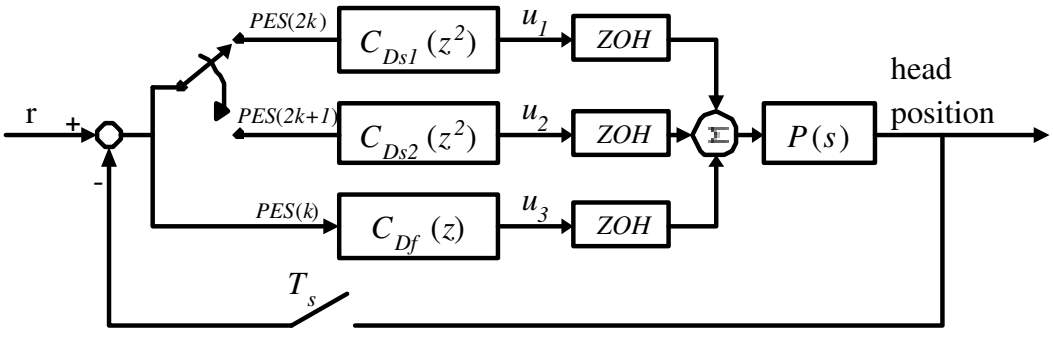

Fig. 5. Multi-rate control with interlacing in parallel form

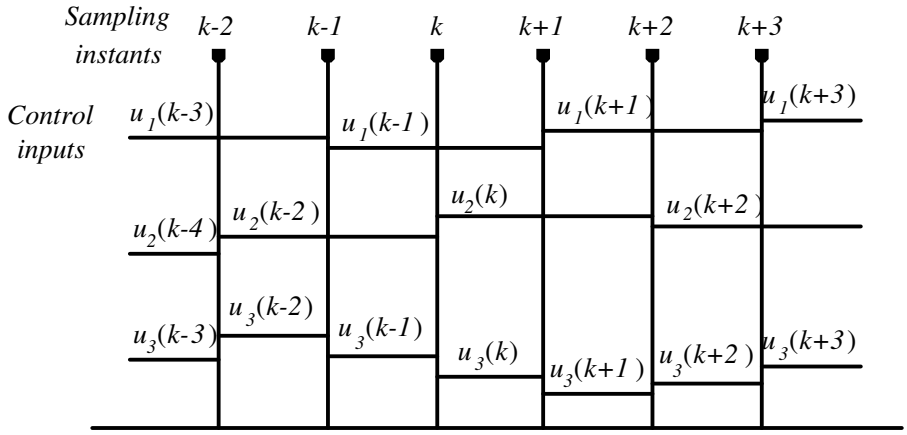

Fig. 6. Time chart of multi-rate control with interlacing

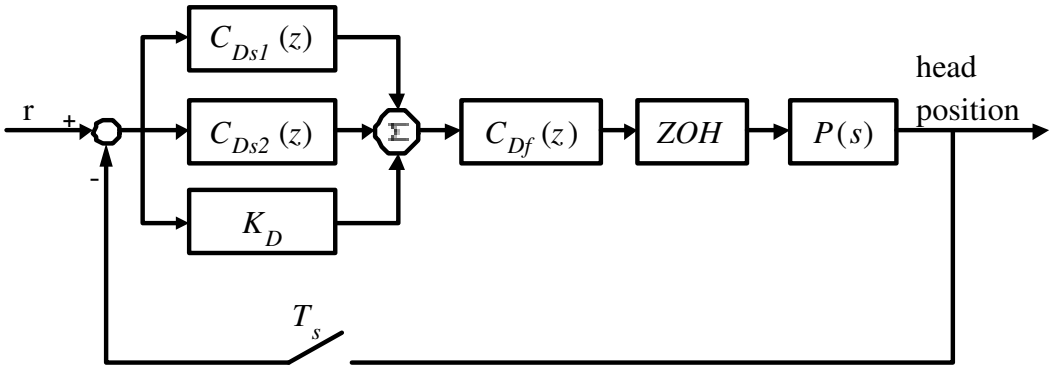

Fig. 7. Implementation of controller using serial decomposition

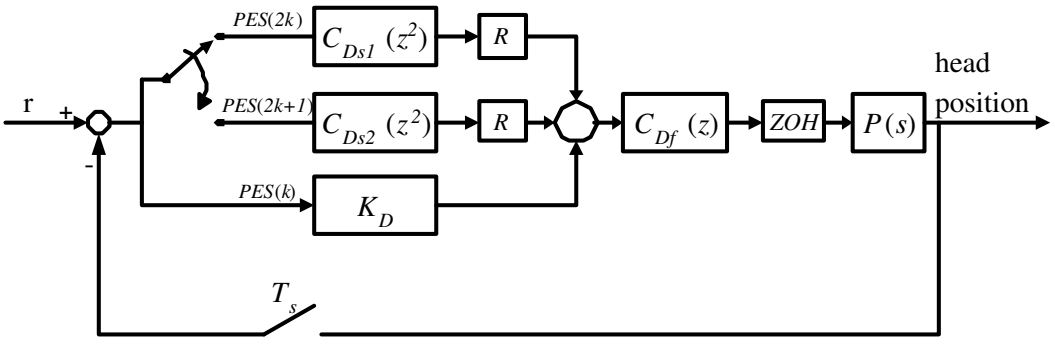

Fig. 8. Multi-rate control with interlacing in serial form

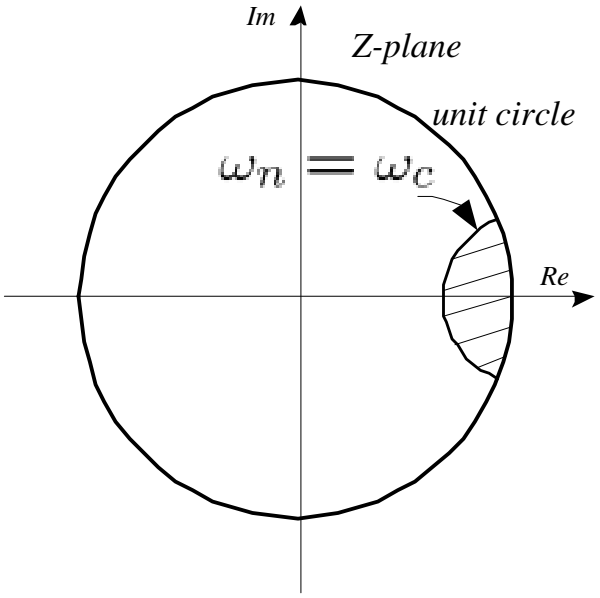

Fig. 9. Boundary of fast modes and slow modes

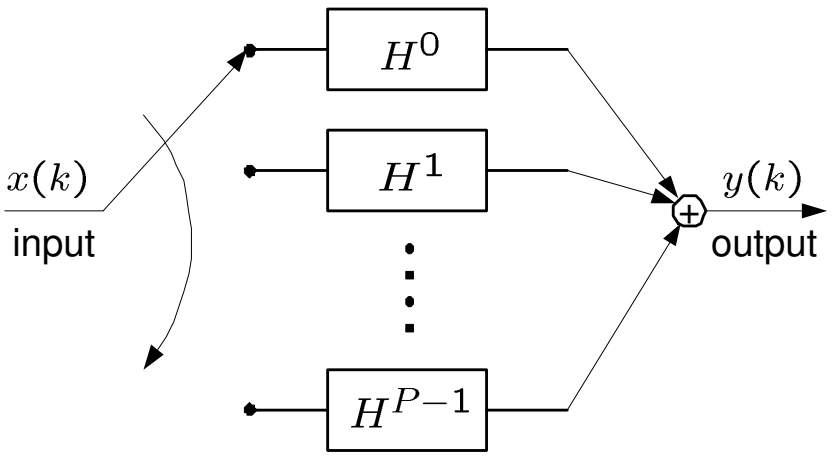

Fig. 10. Switch structure of LPTV system

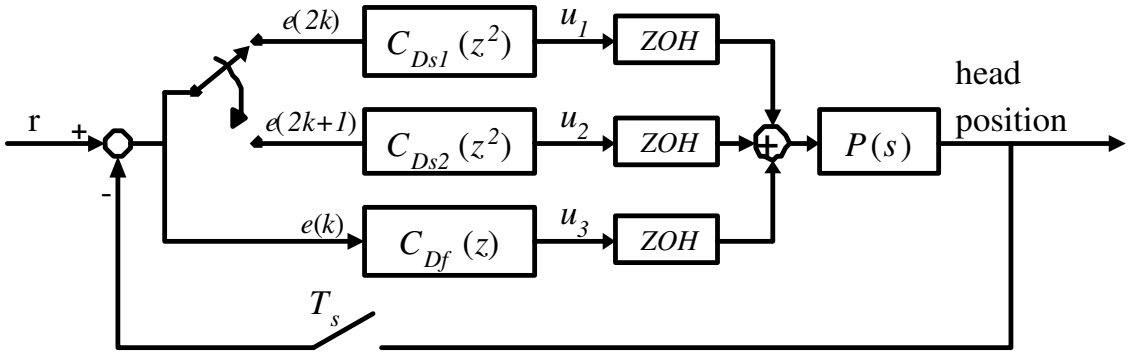

Fig. 11. Multi-rate controller with parallel structure

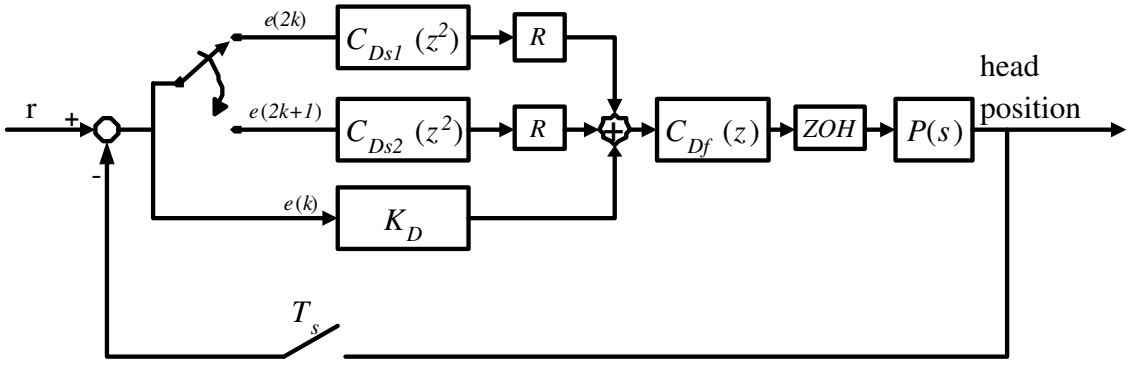

Fig. 12. Multi-rate controller with parallel structure

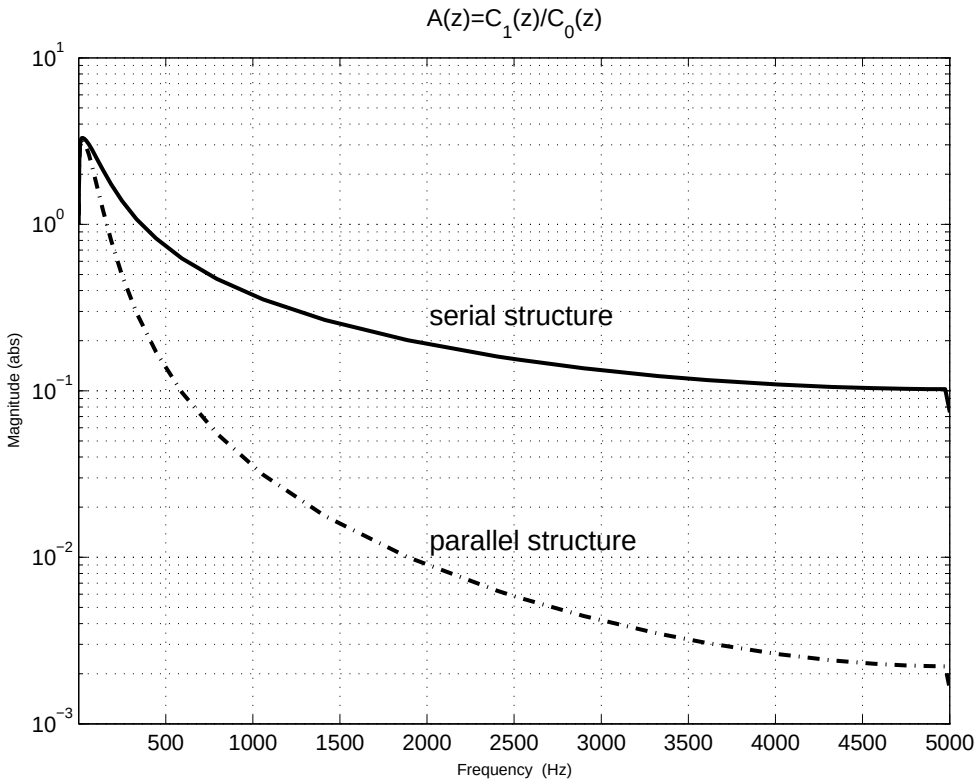

Fig. 13. Frequency response of aliasing indicator $A(z)$

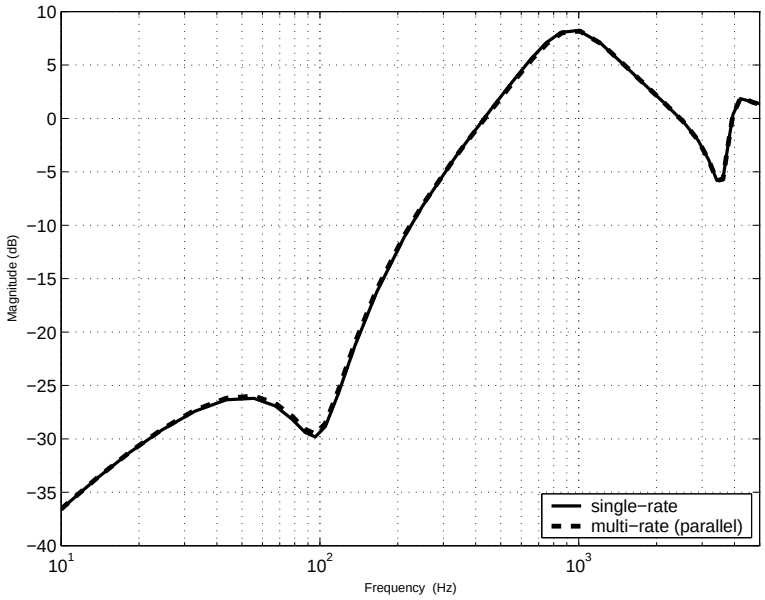

Fig. 14. Sensitivity function for parallel structure

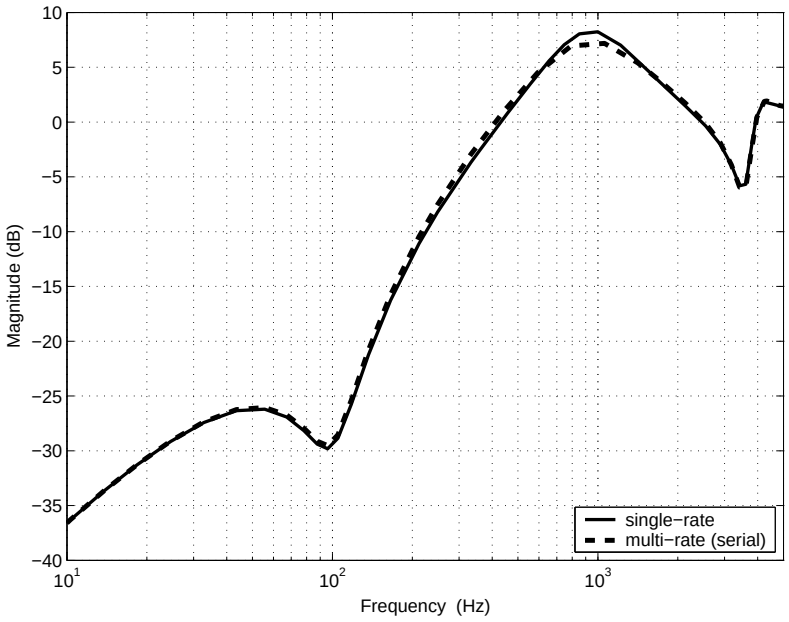

Fig. 15. Sensitivity function for serial structure

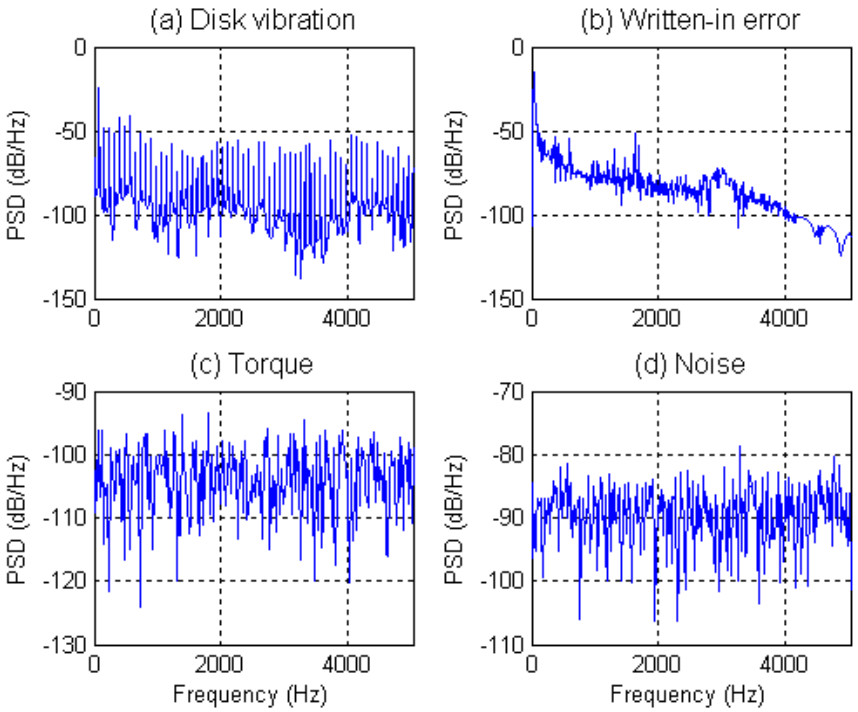

Fig. 16. Power spectrum density of disturbances: (a) disk vibration , (b) servo written-in error (c) windage torque, (d) sensor noise

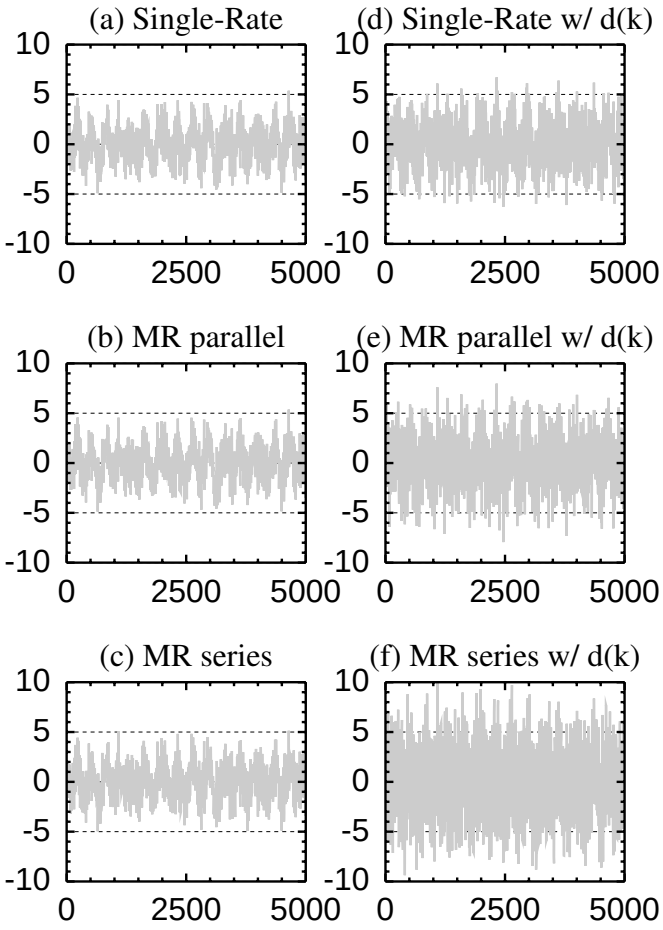

Fig. 17. PES time plots (simulation results): (a) single-rate, (b) parallel multi-rate, (c) series multi-rate, (d) single-rate with $d(k)$, (e) parallel multi-rate with $d(k)$, (f) series multi-rate with $d(k)$

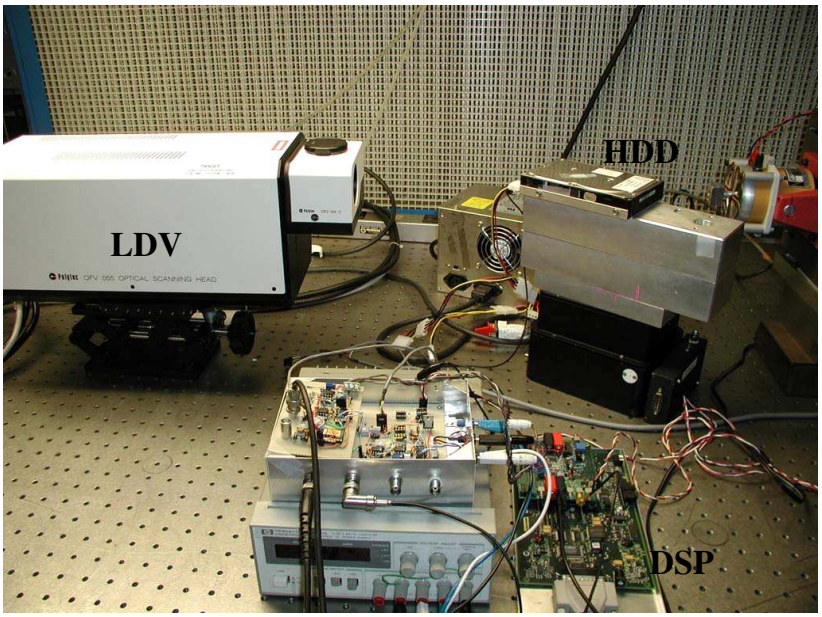

Fig. 18. Experimental setup

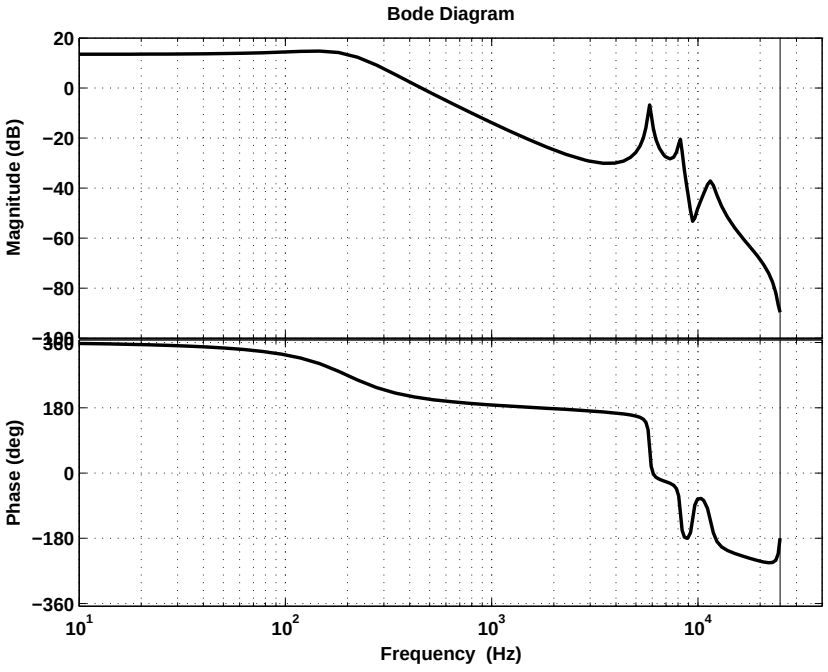

Fig. 19. Frequency response of VCM $P(z)$ (experiment)

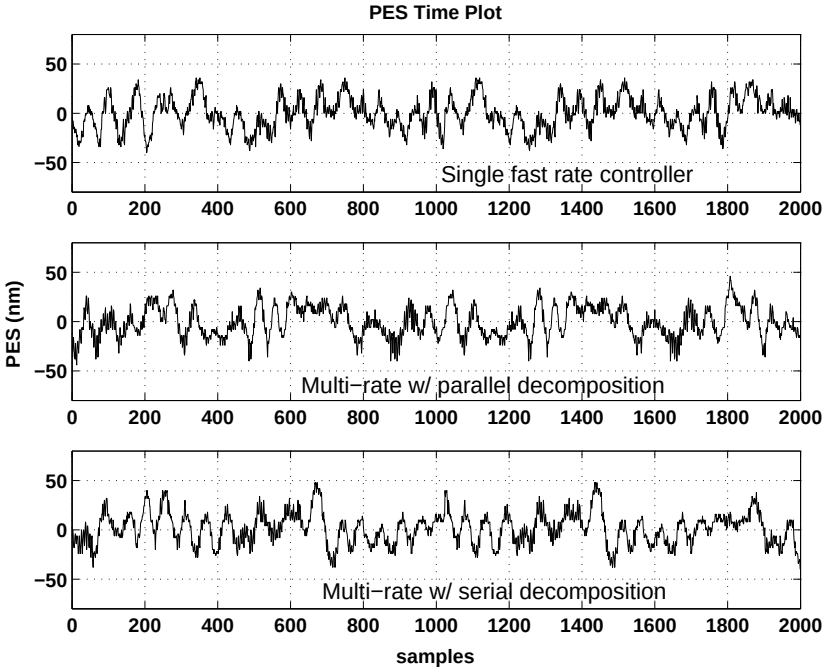

Fig. 20. PES time plots (experimental results)